

MM8512:

Powered by Mobius Microsystems' patented CMOS Harmonic Oscillator (CHO) technology, the MM8512 replaces quartz crystal based oscillators with a monolithic CMOS IC and offers programmable output frequencies and Spread Spectrum Clocking functionality without the use of any mechanical frequency source or PLL.

Features:

- Low Power All-CMOS Temperature Compensated Oscillator
- No quartz or other mechanical resonators or PLL used
- Spread Spectrum output to reduce EMI
- Factory programmable down- and center- spread options
- Factory programmable spread magnitude (0.25 to 6%),
- Factory programmable output frequency (10 to 100MHz)
- Best-in-class Phase Noise and Jitter performance

Electrical Specifications:

VDD=3.0V to 3.6V, T_A=0 to 70°C unless otherwise noted. Typical values are measured at VDD=3.3V, T_A=35°C

Ordering Information:

MM8512	-	40	V3	C	P56	C	D1	±	T
1		2	3	4	5	6	7	8	9

- 1) Mobius Microsystems Part Number
- 2) Output frequency (*programmable*)
- 3) Supply Voltage (*V3: 3.3V*)
- 4) Output Signal Type (*C: CMOS*)
- 5) Package Type (*P56: SMD 5x3.2mm 6pin*)
- 6) Temperature Range (*C: 0 to 70°C*)
- 7) Spread Spectrum Settings (*Please see Table.1 below*)
- 8) Environmental Compliancy (*+: Green, Pb-Free*)
- 9) Tape & Reel (*T: Tape & Reel shipment*)

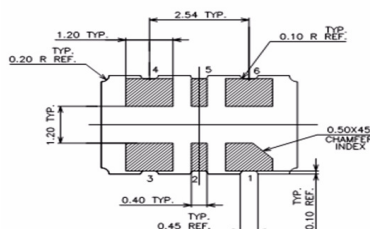
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	VDD		3.0	3.3	3.6	V
Temperature	T _A	Ambient temperature in normal operation	0		70	°C
Input LOW level	V _{IL}				30% x VDD	V
Input HIGH level	V _{IH}		70% x VDD			V
Supply Current	IDD	Active supply current, no output load		14		mA
Quiescent Current	IDDQ	CE=LOW, output disabled		0.2		µA
Output LOW level	V _{OL}	I _{OL} = -8mA			0.45	V
Output HIGH level	V _{OH}	I _{OH} = 8mA	VDD-0.6			V
Output Frequency	F _{OUT}	Factory Programmable. Contact Mobius for frequencies beyond the limit	10		100	MHz
Frequency Stability	F _{TOT}	Total Frequency Stability over temperature, supply variation, aging (1st year at 35°C), shock & vibration. Spread Spectrum turned OFF.		±400		ppm
Rise Time	RT	20% to 80% x VDD. Output load (C _L) = 8pF			2.0	ns
Fall Time	FT	80% to 20% x VDD. Output load (C _L) = 8pF			2.0	ns
Duty Cycle	DC	Clock output duty cycle. Measured at VDD/2, C _L =8pF	45		55	%
Power-up time	t _{on}	Output valid time after VDD meets the specified range		300		µs
Period Jitter	PJ _{RMS}	Total RMS Period Jitter (including random and deterministic) ¹		3		ps _{RMS}
Cycle-cycle Jitter	CJ _{RMS}	Std dev of the max change in the periods of any 2 adjacent cycles ¹		6		ps _{RMS}
Phase Noise	PN	1MHz offset from carrier, F=40MHz, 50Ω termination		-140		dBc/Hz

Note 1. Measured at 40MHz frequency with a 50Ω termination to GND

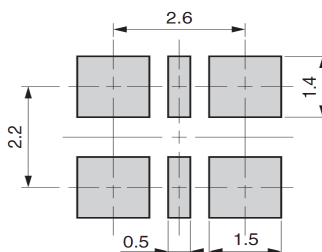
Table.1 Spread Spectrum order codes and settings (Contact factory for more selections)

C1	Center Spread, ±0.25%	C4	Center Spread, ±1%	C7	Center Spread, ±3%	D3	Down Spread, -1.5%	D6	Down Spread, -4%
C2	Center Spread, ±0.5%	C5	Center Spread, ±1.5%	D1	Down Spread, -0.5%	D4	Down Spread, -2%	D7	Down Spread, -6%
C3	Center Spread, ±0.75%	C6	Center Spread, ±2%	D2	Down Spread, -1%	D5	Down Spread, -3%		

Package Drawing:



Recommended Land Pattern:



Pin Assignments:

1	CE	Chip Enable. Device active when CE is HIGH
2	SSOFF	Spread Spectrum Disable. SSC active when SSOFF is LOW
3	GND	Ground
4	OUT	Clock output
5	NC	No Connect
6	VDD	Power Supply. Connect a 0.1µF cap between VDD and GND pins

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